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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q64325

Tsugio TAKAHASHI

Appln. No.: 09/849,362

Group Art Unit: 2832

Confirmation No.: 8102

Examiner: Unknown

Filed: May 07, 2001

For: MATRIX SWITCH CIRCUIT

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

One copy of each of the listed documents is submitted herewith.

1. Japanese Unexamined Patent Application Publication No. 60-201795, published October 12, 1985.
2. Japanese Unexamined Patent Application Publication No. 63-272118, published November 9, 1988.
3. Japanese Unexamined Patent Application Publication No. 7-58808, published March 3, 1995.

Tsugio TAKAHASHI
09/849,362
INFORMATION DISCLOSURE STATEMENT


The present Information Disclosure Statement is being filed: (1) No later than three months from the application's filing date for an application other than a continued prosecution application (CPA) under §1.53(d); (2) Before the mailing date of the first Office Action on the merits (whichever is later); or (3) Before the mailing date of the first Office Action after filing a request for continued examination (RCE) under §1.114, and therefore, no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents, Applicant encloses herewith a copy of a Japanese Office Action dated February 18, 2003 and an English translation of the pertinent portions thereof, which cites such documents and indicates the degree of relevance found by the foreign patent office.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

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Respectfully submitted,


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WASHINGTON OFFICE



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PATENT TRADEMARK OFFICE

Date: May 19, 2003

Ref Q64325

Dispatch date: February 18, 2003

Regarding Claims 1 through 10:

Described in Cited Literature 1 is a device that can realize a large-scale digital space switch LSI because a selector system is configured with a digital space switch and is designed to eliminate unnecessary buffer power.

Described in Cited Literature 2 is a device that is configured with an M input 1 output selector and an LSI digital space switch, and that is designed to eliminate chip area and to eliminate drive capacity.

Described in Cited Literature 3 is a device combined with a selector circuit that realizes a cross-connect to input STS1 signals.

List of Cited Literature

1. Japanese Unexamined Patent Application Publication S60-201795
2. Japanese Unexamined Patent Application Publication S63-272118
3. Japanese Unexamined Patent Application Publication H07-058808

